Graphical Transformation of Non-Ideal OTA Integrator

Paul van der Wagt, July 2010

Graphical transformations are combined with simple algebra to derive open and closed loop parameters of a non-ideal OTA integrator. In one approach the closed-loop response is derived after a few transformations. To the best knowledge of the author it is the fastest way to analyze this archetypical circuit. In a second approach it is shown that the closed-loop response is a superposition of a feedforward response and an ideal feedback response. Their sum features the well-know right-hand *s*-plane zero. The two approaches lead to different open-loop gain definitions, only the first including all loop effects.

The OTA Integrator

Figure 1 shows our Operational Transconductance Amplifier, OTA, integrator circuit, where we assume that biasing is taken care of [1]. Parameters of this circuit as a whole are often referred to as "closed loop." In a way this is misleading, since it is not directly clear how to define the "open loop" yet, as we will find out. We will follow the convention with the understanding that closed-loop means the entire circuit, independent of whether an open loop gain has been identified.

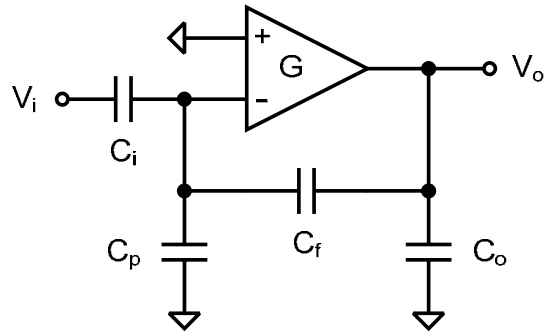

Figure 1. OTA integrator with input, parasitic, feedback, and output capacitances. DC biasing not shown.

Questions to answer: (1) For closed-loop (so complete) circuit, find DC gain, bandwidth (BW), gain-bandwidth product (GBW), and unity-gain bandwidth (UGB); (2) Map this circuit to a feedback block diagram – what are the resulting open-loop gain function, GBW, and UGB? As a first step we simplify Figure 1 to Figure 2, introducing four admittances

$$Y_x = sC_x, x = i, p, f, o. \tag{1}$$

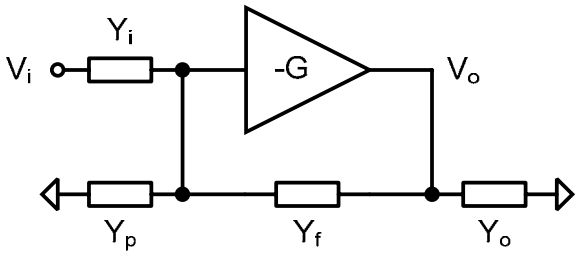

Figure 2. Simplified equivalent of Figure 1.

Graphical Reduction Tools

Figure 3 shows the well-known Thevenin equivalence between a voltage source with series impedance 1/Y and a current source with parallel admittance Y. Repeated application yields the equivalences shown in Figure 4.

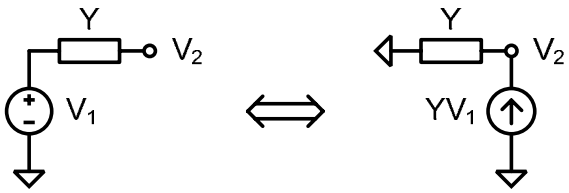

Figure 3. Thevenin equivalent circuits.

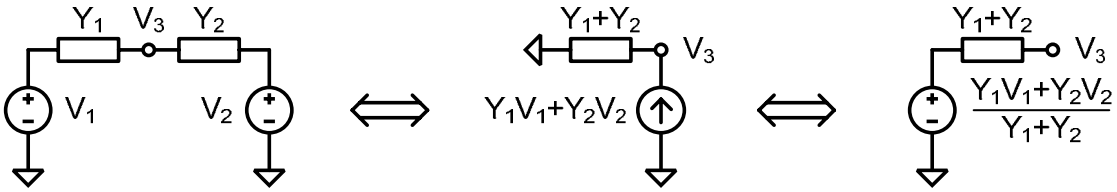

Figure 4. Extended Thevenin equivalent circuits.

We only need one more equivalence. It is shown in Figure 5, and it can be verified easily by comparing the current-voltage equations. The right-hand side has ground references "hidden" in the buffers and it may be interpreted as a two-port, see Figure 6. Although this is well known from linear network theory, the particular drawing style of Figure 5 is usually not employed, but it is very useful to us, as we show in the next two sections.

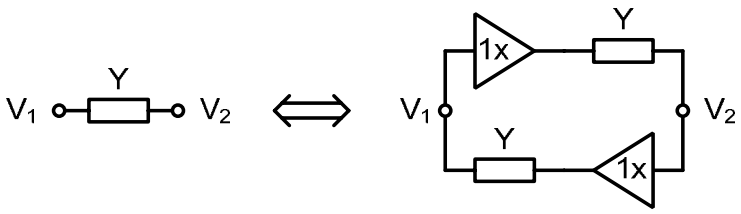

Figure 5. Two-port equivalent of an admittance Y.

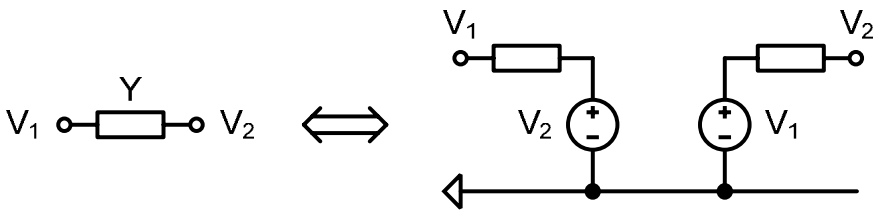

Figure 6. More easily recognized two-port equivalent of admittance Y.

Approach 1: Merge Active and Passive Forward Gains in the Feedback Loop

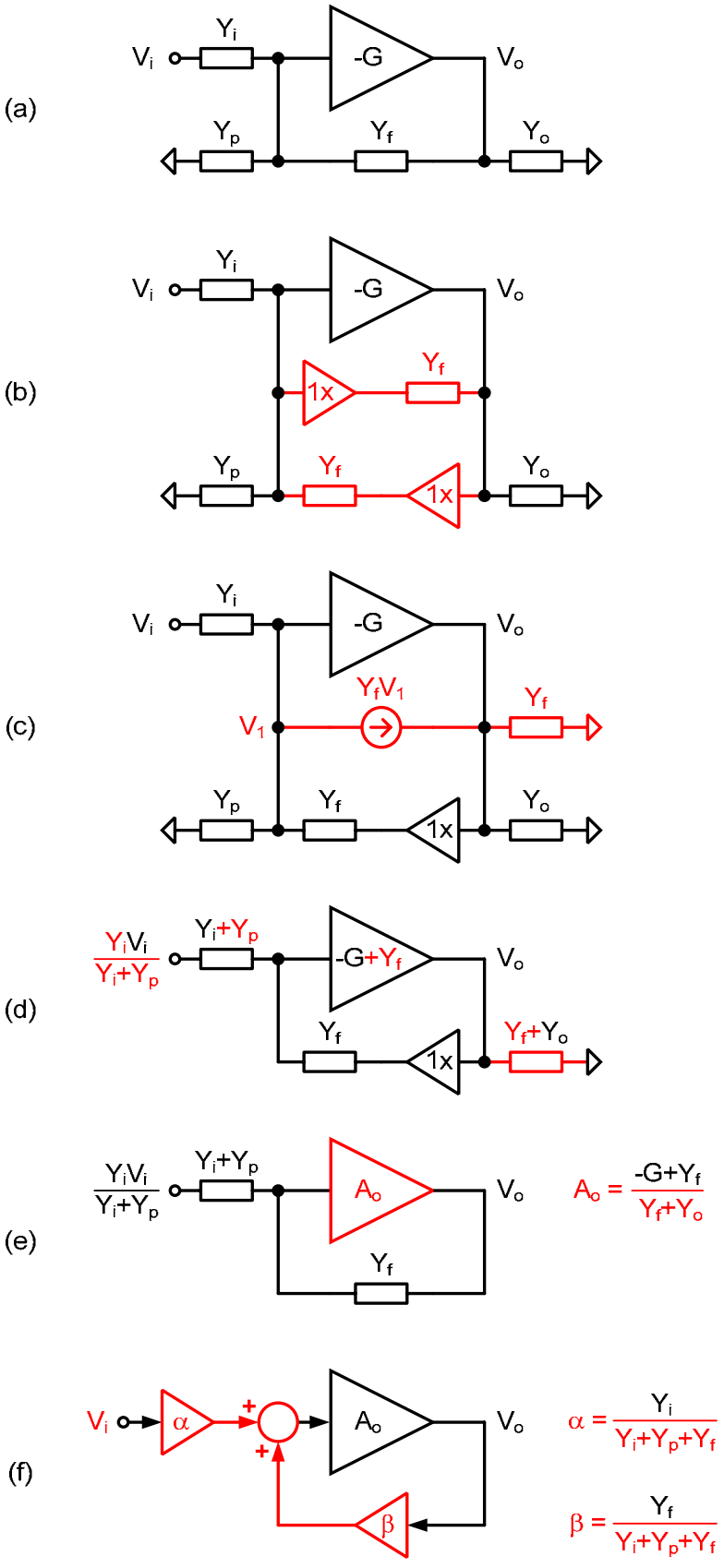

Figure 7. Five-step exact transformation of original circuit into a single standard feedback loop.

In Figure 7 the color red indicates newly introduced elements from one sub-figure to the next. Step one is to apply Figure 5 to the original circuit to give Figure 7(b). We obtain Figure 7(c) after a single use of Figure 3. To get to Figure 7(d), we combine two forward transconductors, combine the parallel admittances Y_f and Y_o at the output, and use Figure 4 on the input side (where V_p = 0 V). Use of Figure 3 converts the tranconductor current source in parallel with the total output admittance into a voltage source with series admittance $Y_f + Y_o$, which can be dropped because it drives the infinite-impedance 1x buffer, after which the 1x buffer is also dropped because A_o has zero output impedance, yielding Figure 7(e). Because of the ideal nature of A_o, Figure 7(f) immediately follows from Figure 7(e). We list the auxilary equations introduced in Figure 7 here.

Open-loop Gain
$$\boxed{A_o(s) = \frac{-G + Y_f}{Y_f + Y_o} = \frac{-G + sC_f}{s(C_f + C_o)}}, \tag{2}$$

"Input Factor"
$$\alpha = \frac{Y_i}{Y_i + Y_p + Y_f} = \frac{C_i}{C_i + C_p + C_f}, \tag{3}$$

Feedback Factor
$$\beta = \frac{Y_f}{Y_i + Y_p + Y_f} = \frac{C_f}{C_i + C_p + C_f}. \tag{4}$$

In addition, βA_o is the loop gain. From standard feedback theory applied to, or elementary analysis of, Figure 7(f), we have for the closed-loop gain

$$\boxed{A_c(s) = \alpha \frac{A_o(s)}{1 - \beta A_o(s)} = -\frac{C_i}{C_f} \frac{1 - \dfrac{sC_f}{G}}{1 + \dfrac{sCC}{GC_f}}}, \tag{5}$$

where

$$CC = C_o(C_i + C_p + C_f) + C_f(C_i + C_p). \tag{6}$$

Evidently (5) has a pole and a zero with frequencies:

LH plane pole frequency
$$f_p = \frac{GC_f}{2\pi CC}, \tag{7}$$

RH plane zero frequency
$$f_z = \frac{G}{2\pi C_f}. \tag{8}$$

The right-hand s-plane zero, $s_z = G/C_f$, in (5) is already visible in the overall transconductance $-G + Y_f$ in Figure 7(d).

Expressions (2, 5) answer our questions. Start with open loop parameters. Since α and β are frequency independent, a constant open-loop GBW$_o$ is given by (2) for frequencies well below the zero frequency:

$$\mathrm{GBW}_o(f) = A_o(2\pi i f)\, f = \frac{G}{2\pi(C_o + C_f)}\ ,\ f << f_z = \frac{G}{2\pi C_f}. \tag{9}$$

For the unity-gain frequency, UGB_o, we find from (2)

$$\mathrm{UGB}_o = \frac{G}{2\pi\sqrt{(C_o + C_f)^2 - C_f^2}} \approx \frac{G}{2\pi(C_o + C_f)}, \text{ if } C_o >> C_f. \tag{10}$$

This makes sense: For $C_f << C_o$, the zero frequency, $f_z = |s_z|/2\pi$, occurs well past the GBW_o and UGB_o equals GBW_o. For this integrator circuit, neither open-loop DC gain or BW are defined.

For the closed loop we have from (5)

$$A_{c,DC} = -\frac{\alpha}{\beta} = -\frac{C_i}{C_f}, \tag{11}$$

$$\mathrm{BW}_c \approx \frac{GC_f}{2\pi CC}\ , \text{ if } C_f^2 << CC \text{ (ignore zero)}, \tag{12}$$

$$\mathrm{GBW}_c \approx \frac{GC_i}{2\pi CC}, \text{ if } C_f^2 << CC \text{ (ignore zero)}, \tag{13}$$

and

$$\mathrm{UGB}_c \approx \mathrm{GBW}_c\ , \text{ if } C_i C_f << CC \text{ (ignore zero) and } A_{V,c,DC} >> 1, \tag{14}$$

The DC closed-loop gain, $A_{c,DC}$, is often moderate, with C_i and C_f in (9) of the same order of magnitude, in which case the second condition of (12) is not fulfilled. In fact, if $C_i < C_f$, $A_{c,DC} < 1$ and UGB_c is not defined. The GBW_c is still the frequency at which the first-order pole roll-off tangent line of the closed-loop frequency response, $A_c(2\pi if)$, crosses unity.

If C_i, C_p, C_f, C_o are all similar in magnitude, the capacitance conditions in (11-13) are reasonably fulfilled, since $CC \sim 5C_f^2 \sim 5C_iC_f$. But from (7,8) the zero frequency is only about 5x the pole frequency.

Approach 2: Exclude Passive Forward Gain from the Feedback Loop

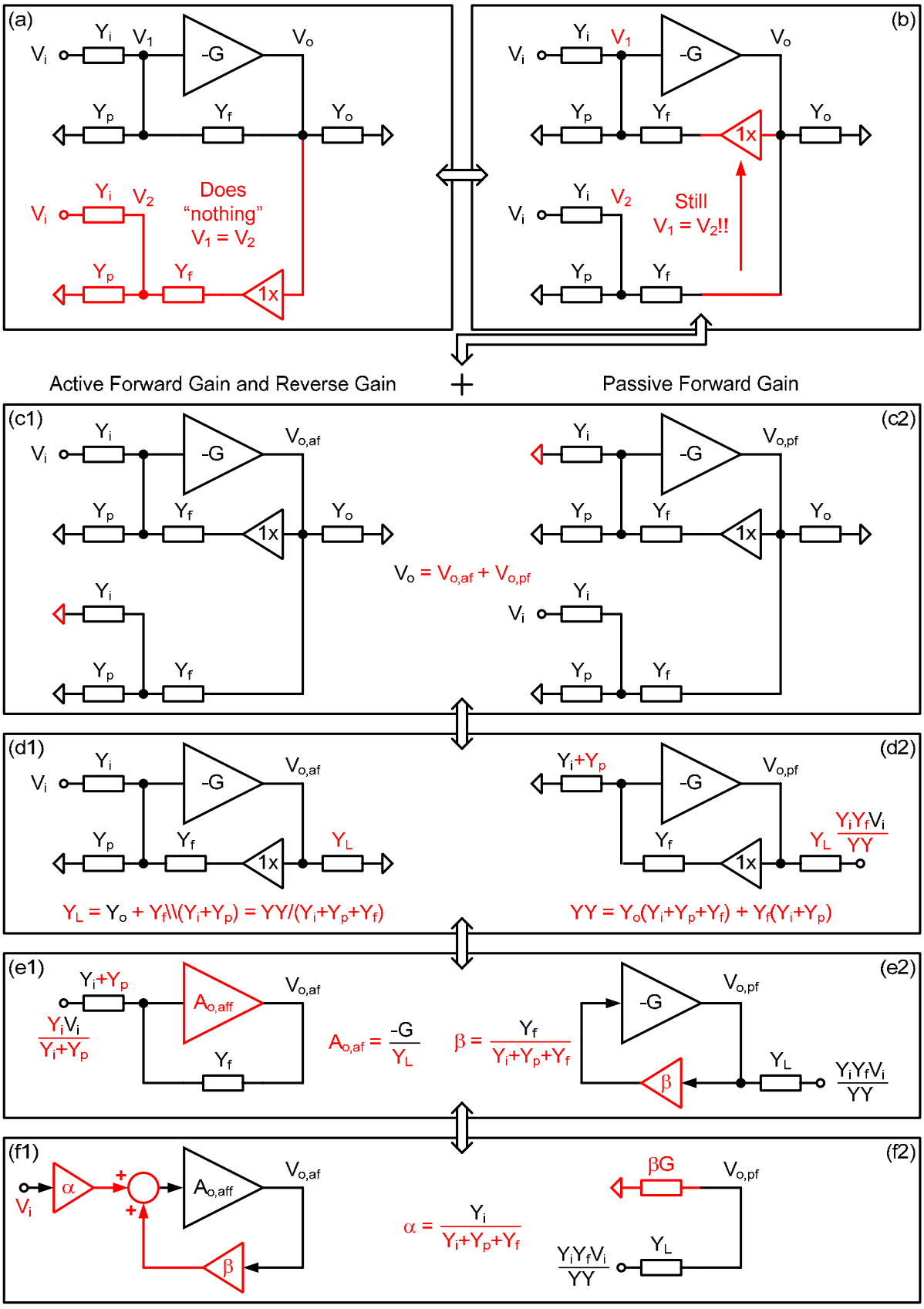

Figure 8. Six-step transformation of circuit response into a sum of an active $V_{o,af}$ and a passive $V_{o,pf}$.

In Figure 8, as before, the color red indicates newly introduced elements. Step one is to add a circuit that does not affect the original circuit, to give Figure 8(a). The "replica" circuit produces a copy, V_2, of the original circuit voltage V_1. In Figure 8(b) we move the 1x buffer from the replica circuit to the original circuit. Because of the infinite input impedance of the ideal transonductor $-G$, this presents the same loading on V_o and therefore all node voltages are unchanged. Since we are dealing with linear circuit response, the two V_i inputs may be activated one at the time and the sum of the resulting outputs, $V_{o,af}$ and $V_{o,pf}$, (or any node voltage responses) is the full circuit response V_o, as depicted in Figure 8(c):

$$\text{Superposition} \qquad V_o = V_{o,af} + V_{o,pf} \,. \tag{15}$$

Figure 8(c1) encodes the response due to intended or forward active forward (AF) gain, involving $-G$, and feedback, involving Y_f, while Figure 8(c2) encodes the response to the unintended or "parasitic" or passive forward (PF) gain due to the bilateral nature of Y_f.

> In computer simulation of feedback loop gain it is common practice to replace the original circuit by the one in Figure 8(c1) with only the active forward gain, then break the loop at the input of the 1x buffer, voltage-drive this input, and observe the returned voltage. This procedure is correct for Figure 8(c1) itself, but ignores the passive forward gain of Figure 8(c2). The correct loop gain for stability analysis may be obtained with a more advanced method. It is used in Cadence Spectre simulator's stb analysis [2].

In Figure 8(d1) the complete load admittance of Figure 8(c1) is combined into Y_L, where "\\" means a series connection, i.e. $Y_1 \backslash\backslash Y_2 = Y_1 Y_2 / (Y_1 + Y_2)$:

$$\text{Load Admittance} \qquad Y_L = Y_o + \frac{Y_f (Y_i + Y_p)}{Y_i + Y_p + Y_f} = \frac{YY}{Y_i + Y_p + Y_f}, \tag{16}$$

where

$$YY = Y_o (Y_i + Y_p + Y_f) + Y_f (Y_i + Y_p) = s\,CC \,. \tag{17}$$

The final two steps to get to Figure 8(f1) are similar to the last steps in Figure 7, and introduce more auxilary equations. Both α and β are still given by (3, 4), but the AFF open-loop gain is

$$\text{Open-loop Gain} \qquad \boxed{A_{o,af} = \frac{-G}{Y_L} = \frac{-G}{sC_L}}, \tag{18}$$

where

$$\text{Load Capacitance} \quad C_L = C_o + \frac{C_f (C_i + C_p)}{C_i + C_p + C_f} = \frac{CC}{C_i + C_p + C_f}, \tag{19}$$

Since there is no loop associated with the PF schematic in Figure 8(f2) $A_{o,pf}$ does not exist.

Closed-loop AF gain is, by inspection of Figure 8(f1):

$$\boxed{A_{c,af}(s) = \alpha \frac{A_{o,af}(s)}{1-\beta A_{o,af}(s)} = -\frac{C_i}{C_f}\frac{1}{1+\dfrac{sCC}{GC_f}}}, \tag{20}$$

where *CC* is given by (6). The closed-loop PF gain is, from Figure 8(f2):

$$\boxed{A_{c,pf}(s) = \frac{\dfrac{sC_i}{G}}{1+\dfrac{sCC}{GC_f}} = -\frac{C_i}{C_f}\frac{-\dfrac{sC_f}{G}}{1+\dfrac{sCC}{GC_f}}}, \tag{21}$$

Consistent with (15) the sum of (20) and (21) is the complete closed-loop gain (5):

$$A_c = A_{c,af} + A_{c,pf}, \tag{22}$$

Again, we answer the original questions, starting with open loop parameters. As (18) is a pure first-order roll-off with real frequency $f = s/2\pi i$, a $\mathrm{GBW}_{o,aff}$ exists independent of frequency and equals $\mathrm{UGB}_{o,af}$:

$$\mathrm{GBW}_{o,af} = \mathrm{UGB}_{o,af} = \frac{G}{2\pi C_L}. \tag{23}$$

For the closed loop we have from (20) and (21)

$$A_{c,af,DC} = -\frac{C_i}{C_f}, \tag{24}$$

$$A_{c,pf,DC} = 0, \tag{25}$$

$$\mathrm{BW}_{c,af} = \frac{GC_f}{2\pi CC}, \tag{26}$$

$$\mathrm{GBW}_{c,af} = \frac{GC_i}{2\pi CC}, \tag{27}$$

and

$$\mathrm{UGB}_{c,af} \approx \mathrm{GBW}_{c,af}, A_{V,c,DC} >> 1, \tag{28}$$

As discussed below (12), $\mathrm{UGB}_{c,af}$ does not exist if $A_{c,DC} < 1$.

Plot

For the sample plot in Figure 9, we assumed values close to those of reference [1]: $G = 0.012\ \Omega^{-1}$, $C_o = C_i = C_p = C_f = 60/\pi = 19.1$ pF, giving $f_p = 20$ MHz and $f_z = 100$ MHz from (7,8).

In order to see the connection between open and closed loop response, it is useful to define the direct gain, which is the gain from input to output with the feedback disabled. From (2,3,6) we have for approach 1:

$$A_d(s) = \alpha A_o(s) = \frac{C_i(-G + sC_f)}{s(C_i + C_p + C_f)(C_f + C_o)} =$$

Direct Gain

$$= -GC_i \frac{1 - \dfrac{sC_f}{G}}{s(CC + C_f^2)} \quad . \tag{29}$$

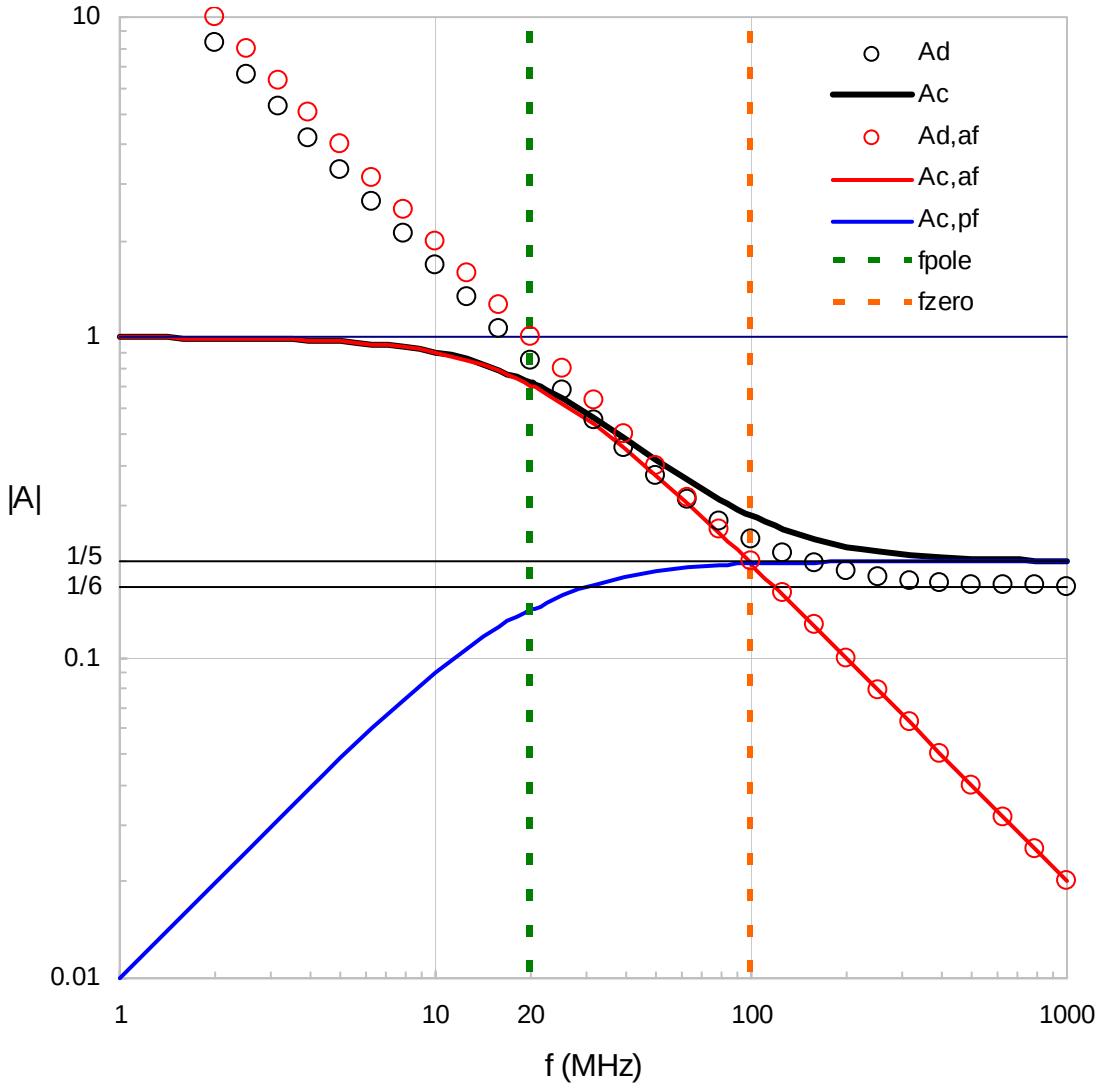

Figure 9. Direct and closed loop gains versus frequency for our two reduction approaches to the OTA integrator.

The closed-loop gain (5) for $f < f_z$ may be written as:

$$A_c(s) \approx -\frac{C_i}{C_f}\frac{1}{\left(1+\frac{sCC}{GC_f}\right)\left(1+\frac{sC_f}{G}\right)} \approx -\frac{C_i}{C_f}\frac{1}{1+\frac{s(CC+C_f^2)}{GC_f}} \ . \tag{30}$$

These gains have the same first-order roll-off tangent lines in a Bode diagram. Since this roll-off happens for A_c for frequencies in between the pole and zero and these are separated by a mere 5x, see (7,8), truly parallel sections are not observed in Figure 9.

For approach 2, the direct gain from (18,19) is:

$$\text{Direct Gain} \qquad A_{d,af} = -\frac{GC_i}{sCC} \ , \tag{31}$$

Figure 9 is based on (29,5,31,20,21,7,8).

Notes and References

[1] K. Bult and G. J. G. M. Geelen, “A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain,” *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379-1384, Dec. 1990.

[2] M. Tian, V. Visvanathan, J. Hantgan, and K. Kundert, “Striving for Small-Signal Stability,” *IEEE Circuits and Devices Magazine*, vol. 17, no. 1, pp. 31-41, Jan. 2001.